REMARKS

After entry of this Amendment, claims 32-34, 37-66, and 70-90 will be pending. Claim 39 has been amended to clarify the scope of the invention and new claim 90 has been added. Support for the claim amendment and new claim may be found, e.g., on page 2, line 18 – page 3, line 8, as well as in Figs. 4A-4D and 5A-5D and related text. No new matter has been added. Applicant notes with appreciation the Examiner's allowance of claims 71-76, 80-84, 87, and 88.

Rejection of claims under 35 U.S.C. § 103

Claims 32-34, 37, 41, 42, 44-48, 65, 66, 70, 77-79, 85, and 86 are rejected under 35 U.S.C. § 103(a) as being obvious over N. Sugii, et al., "Role of $Si_{1-x}Ge_x$ Buffer Layer on Mobility Enhancement in a Strained-Si n-Channel Metal-Oxide-Semiconductor Field-Effect Transistor," *Appl. Phys. Lett.*, Vol. 75, No. 19, pp. 2948-2950 (1999) ("Sugii") in view of U. S. Patent Application Publication No. 2004/0262631A1 to Fitzgerald ("Fitzgerald").

The Examiner relies on Sugii to teach all of the limitations of independent claim 32, except for a first strained layer being compressively strained. The Examiner relies on Fitzgerald to supply this feature, stating that it would have been obvious to one of ordinary skill in the art to modify the teachings of Sugii with those of Fitzgerald to "provide a process that allows controlled relaxation of mismatched semiconductor layers so that many different semiconductor materials can be created on common substrates."

However, the teachings of Sugii and Fitzgerald are utterly incompatible, as even the Examiner's reasoning for the combination suggests. Sugii seeks to fabricate intentionally lattice-mismatched structures incorporating strained Si layers on SiGe while controlling surface roughness to increase mobility in strained Si MOSFETs. *See* Sugii, page 2948, first paragraph and page 2950, right column, first full paragraph. In contrast, Fitzgerald seeks to fabricate relaxed graded GeSi buffer layers (terminating with pure Ge) in order to enable subsequent lattice-matched growth of III-V layers such as GaAs. *See* Fitzgerald, paragraphs [0004] and [0044]. The Examiner refers to paragraph [0006] of Fitzgerald, which underscores the fact that Fitzgerald seeks relaxation of his layers, not mobility-enhancing strain as does Sugii. While Fitzgerald does disclose the incorporation of compressive strain into his GeSi graded layers, such strain is only incorporated into his layer at his growth temperature of 550 °C—at room temperature, the final structure is "nearly stress-free." *See* Fitzgerald, paragraphs [0032] and

[0041]. Thus, each of the references teaches against the other: Sugii seeks large amounts of strain to enhance mobility while Fitzgerald seeks to eliminate strain in his final structures.

Moreover, Fitzgerald only incorporates compressive strain in his structure to offset deleterious tensile strain due to the high coefficient of thermal expansion of pure Ge. *See* Fitzgerald, paragraphs [0040]-[0041]. If Fitzgerald's method were combined with the teachings of Sugii, one of two scenarios is possible:

1. Sugii's structure with his strained Si layer could be combined with the incorporation of compressive strain of Fitzgerald. As Fitzgerald intends, Fitzgerald's compressive strain would offset the tensile strain of Sugii's strained Si layer, lessening or eliminating the very factor that provides Sugii with "low effective mass and high mobility." *See* Sugii, page 2948, first paragraph. Thus, one of skill in the art would not combine the teachings of Fitzgerald with those of Sugii, as Sugii's device would become inoperative for its intended purpose.
2. Sugii's structure without a strained Si layer could be combined with the incorporation of compressive strain of Fitzgerald. However, Fitzgerald teaches against such a scheme, as he only incorporates compressive strain to offset deleterious tensile strain. In the absence of a strained Si layer in Sugii's structure, there is only relaxed $Si_{1-x}Ge_x$ with x=0.2 or 0.3, which one of skill in the art would not modify with the teachings of Fitzgerald.

In either scenario, one of skill in the art would not combine the teachings of Sugii and Fitzgerald. To do so would either render Sugii's structure inoperative or contradict the express teachings of Fitzgerald.

Further, even if one did combine the teachings of Sugii and Fitzgerald, one would render Sugii's device inoperative and would still fall outside the bounds of independent claim 32. Fitzgerald's sample D with incorporated compressive strain has a surface roughness of 24.2 nm. *See* Fitzgerald, Fig. 2. Sugii's structures have surface roughnesses of 0.7-0.9 nm, and he teaches that such roughness must be further controlled to "further increase mobility in strained-Si MOSFETs." *See* Sugii, page 2949, final paragraph and page 2950, right column, first full paragraph. Thus, one of skill in the art would not incorporate the method of Fitzgerald, with its concomitant high surface roughness, into the structure of Sugii since it would degrade the performance of Sugii's devices. Sugii seeks to eliminate surface roughness, not utilize a method that would grossly increase it. *See* Sugii, page 2950, right column, lines 2-4. Finally, the

incorporation of the high surface roughness of Fitzgerald would remove Sugii's structure from the boundaries defined by independent claim 32, which require a first strained layer having an average surface roughness of no more than approximately 2 nm. All of Fitzgerald's structures exceed his requirement by at least an order of magnitude. *See* Fitzgerald, Fig. 2.

Therefore, we submit that, for at least these reasons, independent claim 32 and claims depending therefrom are patentable over the cited art.

Regarding dependent claims 45 and 78, the Examiner claims that Sugii discloses providing a relaxed layer or strained layer by wafer bonding. Applicant submits that neither Sugii nor Fitzgerald teaches or suggests providing any layer by wafer bonding. As disclosed in the instant Specification, wafer bonding is a technique that enables the transfer of a layer from one substrate to another after the two substrates are bonded together. *See* Specification, Figs. 4A-4D and related text. In contrast, Sugii and Fitzgerald provide all of their layers by growth. *See* Sugii, Fig. 1 and related text and Fitzgerald, paragraphs [0022] amd [0024]-[0029]. Such growth processes are vastly different from wafer bonding, and do not involve physical attachment of pre-existing layers.

Therefore, we submit that, for these additional reasons, dependent claims 45 and 78 are patentable over the cited art.

Claims 38 and 40 are rejected under 35 U.S.C. § 103(a) as being obvious over Sugii in view of Fitzgerald, and further in view of Mizuno et al., "Electron and Hole Mobility Enhancement in Strained-Si MOSFET's on SiGe-on-Insulator Substrates Fabricated by SIMOX Technology," *IEEE Electron Device Letters*, Vol. 21, No. 5 (May 2000) ("Mizuno").

The Examiner relies on Sugii and Fitzgerald to teach all of the limitations of dependent claim 38, except for providing an insulating layer disposed beneath a first strained layer. The Examiner relies on Mizuno to supply this feature, stating that it would have been obvious to one of ordinary skill in the art to modify the teachings of Sugii with those of Mizuno to "form a FET structure with low parasitic capacitance of source/drain junction, high carrier mobility, and simple isolation."

In the Response to Office Action submitted on August 15, 2007 ("the August 2007 Response"), Applicant argued in detail against the identical combination of references (in a

rejection of independent claim 39), including a submission of evidence demonstrating that the Examiner's combination of Sugii and Mizuno is improper. The Examiner did not respond to Applicant's evidence, and the relevant portion of the August 2007 Response was repeated in the Response to Office Action submitted on October 30, 2007 ("the October 2007 Response"). The Examiner has still not responded to Applicant's evidence regarding the incompatibility of Sugii and Mizuno, so Applicant herein repeats the relevant portion of the August 2007 Response for the Examiner's convenience and respectfully requests consideration thereof:

> For the reasons that follow, we respectfully submit that the proposed combination would not be made by one of skill in the art, and, furthermore, that the function of Sugii's device is destroyed by the combination with Mizuno. Sugii specifically forms his strained Si-based structures on relaxed $Si_{1-x}Ge_x$, where x is 0.2 or 0.3, corresponding to 20% or 30% Ge. *See* Sugii, p. 2948, paragraph 3. Mizuno forms his structure by implanting oxygen ions into relaxed $Si_{0.9}Ge_{0.1}$ (i.e., 10% Ge) and annealing at 1350 °C. *See* Mizuno, p. 230, section II. Device Structure and Fabrication Processes, paragraph 1. The combination of the structure of Sugii with the method of Mizuno would result in the high temperature annealing of SiGe layers having 20% or 30% Ge at 1350 °C. However, this extreme temperature is higher than the melting point of SiGe alloys containing 20-30% Ge, as expressly shown by the solidus line of the Si-Ge phase diagram. *See* S. K. Ghandi, VLSI Fabrication Principles: Silicon and Gallium Arsenide, John Wiley & Sons, Inc.: New York, p. 74 (1994) [attached to the August 2007 Response as Appendix 1]. The melting point of SiGe alloys containing 20-30% Ge falls between approximately 1200 °C and 1275 °C. Thus, it would not be obvious to one of ordinary skill in the art to apply the method of Mizuno to the structure of Sugii, as layers of Sugii's structure would melt and be rendered inoperative. Notably, Mizuno and his co-workers themselves admitted, in a subsequent publication, that their method is not usable with SiGe having a high Ge content. Mizuno et al. stated that "the melting point of SiGe layers with high Ge content is too low for the high temperature annealing of the SIMOX process," and that the Ge content of layers compatible with the process is limited to be lower than 14%. *See* p. 601, left column, paragraph 3 of T. Mizuno, et al., "Relaxed SiGe-on-Insulator Substrates without Thick SiGe Buffer Layers," Appl. Phys. Lett., Vol. 80, No. 4, pp. 601-603 (2002) [attached to the August 2007 Response as Appendix 2].
>
> Thus, one of ordinary skill in the art would not combine the structures of Sugii with the methods of Mizuno.

See the August 2007 Response, page 12.

In rejecting dependent claim 40, the Examiner contends that Mizuno (page 230, 2nd column) discloses that the step of providing an insulator comprises wafer bonding. Again, in the October 2007 Response, Applicant traversed an identical rejection of claim 89 and the Examiner

has not specifically responded. Applicant herein repeats the relevant portion of the October 2007 Response for the Examiner's convenience and respectfully requests consideration thereof:

> Applicant submits that Mizuno does not teach or suggest providing an insulator layer by wafer bonding. As disclosed in the instant Specification, wafer bonding is a technique that enables the transfer of a layer from one substrate to another after the two substrates are bonded together. *See* Specification, Figs. 4A-4D and related text. In marked contrast, Mizuno discloses formation of a buried SiO_2 layer inside an $Si_{0.9}Ge_{0.1}$ layer on a single wafer by the Separation-by-Implanted-Oxygen ("SIMOX") technique. *See* Mizuno, p. 230, abstract and right column. Via SIMOX, Mizuno forms his SiO_2 layer by implantation and annealing rather than by wafer bonding... Indeed, the process used by Mizuno is vastly different from wafer bonding. Whereas wafer bonding involves physical attachment to a pre-existing layer, Mizuno's process builds that layer internally.

See the October 2007 Response, page 10.

Therefore, we submit that, for these additional reasons, dependent claims 38 and 40 are patentable over the cited art.

Claims 43, 53, and 70 are rejected under 35 U.S.C. § 103(a) as being obvious over Sugii in view of Fitzgerald, and further in view of the Examiner's remarks. Claims 49-52, 54, and 59-64 are rejected under 35 U.S.C. § 103(a) as being obvious over Sugii in view of Fitzgerald, and further in view of A. G. O'Neill, et al., "SiGe Virtual Substrate N-Channel Heterojunction MOSFETs," Semicond. Sci. Technol., Vol. 14, pp. 784-789 (1999) ("O'Neill 1999"). Claim 55 is rejected under 35 U.S.C. § 103(a) as being obvious over Sugii in view of Fitzgerald, and further in view of O'Neill 1999 and A. G. O'Neill, et al., "Deep Submicron CMOS Based on Silicon Germanium Technology," IEEE Trans. Electron Dev., Vol. 43, No. 6, pp. 911-913 (1996) ("O'Neill 1996"). Claim 56 is rejected under 35 U.S.C. § 103(a) as being obvious over Sugii in view of Fitzgerald, and further in view of O'Neill 1996. Claims 57 and 58 are under 35 U.S.C. § 103(a) as being obvious over Sugii in view of Fitzgerald, and further in view of O'Neill 1996 and the Examiner's remarks.

We submit that these claims are patentable for the same reasons independent claim 32, from which they depend, is patentable.

Claims 39 and 89 are rejected under 35 U.S.C. § 103(a) as being obvious over U.S. Patent No. 6,765,227 to Yu et al. ("Yu") in view of Sugii. Yu appears to disclose a silicon-on-

insulator ("SOI") structure with a silicon-germanium channel. *See* Yu, Fig. 1 and related text. The Examiner relies on Yu to teach all of the limitations of independent claim 39 except for a first strained layer having an average surface roughness of no more than approximately 2 nm, relying on Sugii to supply this feature.

Yu, however, is both incompatible with and teaches against a first strained layer consisting essentially of Si, as recited in amended independent claim 39. Yu forms a strained silicon-germanium layer 66 on silicon substrate 64. *See* Yu, column 3, lines 51-62. Since Yu's substrate 64 is silicon, a strained layer consisting essentially of Si cannot be fabricated thereon. Yu's silicon-germanium layer 66 is only strained due to lattice mismatch between it and the silicon of substrate 64. Thus, a strained layer consisting essentially of Si would have no strain in the structure of Yu. Further, Yu teaches against an active layer consisting essentially of Si, even if one could fabricate one in the structure of Yu. Yu discloses that carriers in his silicon-germanium layer have much higher mobility than those in silicon channels, and that the performance of his device 10 is increased by virtue of the silicon-germanium channel. *See* Yu, column 3, lines 13-23. Thus, the substitution of a silicon layer in the structure of Yu, even if it were possible, would not provide Yu's expressly stated advantages, and one of skill in the art would not make the Examiner's proposed combination.

Moreover, regarding new dependent claim 90, Yu's structure is utterly incompatible with the requirements thereof. Claim 90 requires a layer of SiGe in contact with an insulator layer over a substrate. Yu expressly teaches a structure with lower silicon layer 24 in contact with buried oxide layer 16, stating that such a silicon layer is necessary to help form an oxide layer used to fabricate wafer 12. *See* Yu, Fig. 1 and related text and column 3, lines 31-33. Thus, the method of Yu could not be properly performed with a layer of SiGe in contact with an insulator layer.

Therefore, we submit that, for at least these reasons, independent claim 39 and claims depending therefrom are patentable over the cited art.

CONCLUSION

In light of the foregoing, Applicant respectfully submits that all claims are now in condition for allowance.

Applicant believes that no additional fees are necessitated by the present Response. However, in the event that any additional fees are due, the Commissioner is hereby authorized to charge any such fees to Deposit Account No. 07-1700.

If the Examiner believes that a telephone conversation with Applicant's attorney would expedite allowance of this application, the Examiner is cordially invited to call the undersigned.

Respectfully submitted,

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